# IMPROVING THE CAD OF SRD FREQUENCY MULTIPLIERS

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## ABSTRACT

A method for improving the efficiency of CAD of SRD frequency multipliers is proposed. By abating the nonlinearity of the model of the diode to an appropriate extent, the simulation and optimization of SRD frequency multipliers can be carried out faster and easier. Simulation results are compared with experimental results.

## INTRODUCTION

Step recovery diodes (SRDs) are strongly nonlinear two terminal devices, which are used as comb generators in measurement equipment and as harmonic generators in radios for terrestrial communications, satellite communications, TVRO, and mobile communications. Input frequencies could extend down to 10 MHz and output frequencies up to 94 GHz [1][2]. With proper modeling of the diode, SRD frequency multipliers can be analyzed and optimized with the aid of computers, using harmonic-balance methods [1]. However, due to the very strong nonlinearity of the diode and the difficulty of its modeling, the efficiency of the computer aided design is somewhat low.

In order to improve the efficiency of CAD of SRD frequency multipliers, we have investigated the modeling of the diode and features of SRD frequency multipliers. The results show that abating the nonlinearity of the model of the diode to some extent while optimizing the circuit does not change the characteristics of the circuit radically. On the other hand, the efficiency of the CAD of this kind of circuit is greatly improved and the analysis itself is more easily and faster accomplished.

In this paper, the method of abating the nonlinearity of the model is proposed and the simulation results with different degrees of nonlinearity of the model are compared. Finally, the experimental results are compared with simulation results.

## NONLINEARITY OF SRD

The step recovery diode (SRD), which is also called elsewhere the snap-off diode or charge storage diode, was first recognized in the early 1950's. The diode was modeled in a way that it behaves as a two-state capacitor of large capacitance (diffusion $C_f$) under forward charge storage state and small capacitance (the depletion capacitance $C_r$) under reverse storage state, with zero switching time between states, as shown in Figure 1. Analyses of resonant and nonresonant circuit performance using this model describe the first-order diode behavior very well [3][4].

Nevertheless, the forward state capacitance, which is a diffusion capacitance determined by a large number of free carriers in a finite volume, can not physically be infinite. The transition time, in which an SRD switches between forward and reverse states, can not be zero, either. The transition process can be described

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by a parabolic function, which is determined by the two state capacitance [1]. The characteristic of the diode, illustrated in Figure 2, shows that the smaller is the forward capacitance, the weaker is the nonlinearity of the model. This highly nonlinear capacitance characteristic is also accompanied by a highly nonlinear shunt resistance which depends on the forward bias voltage and RF input power. Therefore, the degree of abatement depends on how much $C_f$ is changed, and the operation condition of the diode

Furthermore, we investigate the effect of the abatement on the circuit characteristics. Through the dc measurement on a step recovery diode HP-0580-0835 [1], we know that the forward charge storage state capacitance ($C_f$) is about 100 nF, while the depletion capacitance ($C_r$) is about 0.3 pF. However, according to [5], in high frequency operation the effective capacitance of an SRD at forward charge storage state increases typically by three orders of magnitude from $C_r$. Using the equivalent circuit in Figure 1 to calculate the input impedance at forward charge storage state, we can see that, when the fundamental frequency is high enough, e.g. 1 GHz or higher, and $C_f$ larger than 0.1 nF, $C_f$ actually does not contribute much to the input impedance with typical parasitic parameters $C_p$ = 0.2 pF, $R_s$=1.3 ohm and $L_p$ = 1 nH. And at reverse bias state, the characteristic of the diode depends only on the depletion capacitance $C_r$. Therefore, if we change $C_f$ to an appropriate lower value according to the used fundamental frequency, the characteristic of the circuit will not be radically changed. However, as we shall see in the following simulations, the simulation of the circuit is much faster and easier.

## SIMULATIONS OF SRD FREQUENCY MULTIPLIERS

Based on the SRD model proposed by Zhang and Räisänen [1], the simulation is directly done with commercial circuit simulator, the HP Microwave and RF Design System (MDS), on a HP workstation (HP 85180).

A 10 ×12.5 GHz SRD frequency multiplier illustrated in Figure 3 is simulated using harmonic balance analysis. A large voltage signal source corresponding to an input power of 13 dBm at 1.25 GHz is used for the harmonic balance simulation. At first, the circuit is optimized for a high conversion efficiency with $C_f$ equal to 0.1 nF. Then the circuit is refined by an experiment. Thereafter, the harmonic balance analyses with swept bias voltage are carried out with $C_f$ equal to 0.1 nF and 100 nF and compared with the experiment.

The simulation results are shown in Figure 4. It can be seen that the shapes of these line pairs are essentially the same. The lines with different $C_f$ are just shifted to the right or left of the other. The conversion efficiency is a little lower with lower $C_f$, which corresponds to weaker nonlinearity of the model. The shifting of lines is partially due to the different degree of the nonlinearity. In a strongly nonlinear circuit, the low-order mixing frequencies generated by high-degree nonlinearity can not be neglected readily; thus, the excitation of a strongly nonlinear circuit may offset the dc operating point.

On the other hand, the computational resources used for different $C_f$ are listed in the following table.

| $C_f$ (nF) | CPU (second) | Virtual Memory Used (MB) |
|---|---|---|
| 100 | 3690 | 3.15 |
| 0.1 | 1104 | 3.15 |

It obviously indicates that the computation time is much less for lower $C_f$ than that for higher $C_f$. The comparison is made under the condition of the same memory used, as can be seen in the table. Furthermore, it should be pointed out that the simulation with higher $C_f$ shows more trouble in convergence, especially in the case of inappropriate initial conditions.

## EXPERIMENTS

A 10 ×12.5 GHz SRD frequency multiplier is realized with microstrip circuits and the diode of HP ceramic packaged step recovery diode HP-5082-0835. The input circuit is used for impedance matching between the 50 ohm source and the low impedance of the diode. The output circuit consists of a section of transmission line, a gap, and a separate microstrip bandpass filter. The input signal is a 1.25 GHz sinusoidal signal at the power level of 13 dBm. The dc bias voltage is fed through a bias tee. The output power is measured using a spectrum analyzer (Tektronix 2782).

The experiment is carried out by changing the bias voltage and recording output power at the 10th harmonic. The conversion efficiency is calculated by dividing the output power by the available power at the input port. The measurement results are shown in Figure 5. The points connected with dashed-lines represent cases where the output signal shows spurious behavior, caused by spurious oscillations in the circuit.

Figure 5 shows that the conversion efficiency varies with bias voltage in a similar way as in the above simulation. The lower experimental efficiency than the calculated result is expected due to the loss of the circuit.

It should be noted that the parasitics due to mounting the packaged diode have been neglected in the simulations. However, both the simulation and experiment show that the circuit is quite sensitive to the length of the transmission line between the diode and gap in the output circuit, which is closely related to the mounting structure of the diode. Therefore, the effects of diode mounting structure might not be neglected in more accurate analyses. Numerical electromagnetic analyses of the effects of the diode mounting structure should be done for better modeling of the multiplier.

## CONCLUSION

The CAD of SRD frequency multipliers can be made more efficient and easier to accomplish by the method of abating the nonlinearity of the model of SRD in the simulation. The experiment shows that the simulated results can be used to guide the multiplier design very well to achieve a high conversion efficiency. An efficiency of more than 2% was achieved at 12.5 GHz with a 10th harmonic multiplier using microstrip circuits.

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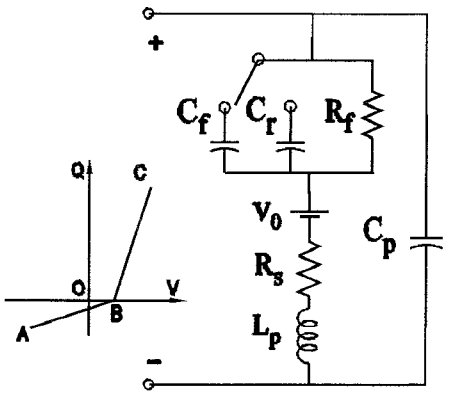


**Figure 1. Conventional model of SRD.**

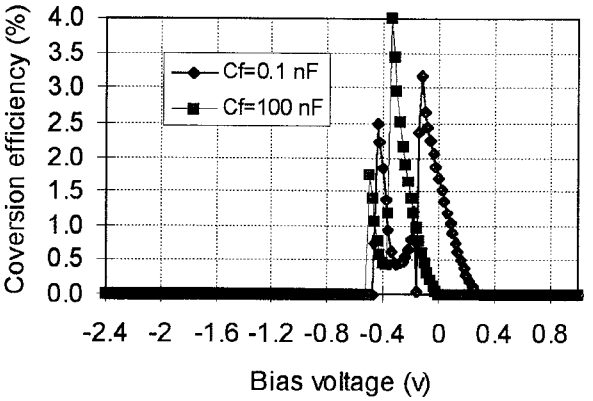


**Figure 4. Simulated results of conversion efficiency vs. bias voltage.**

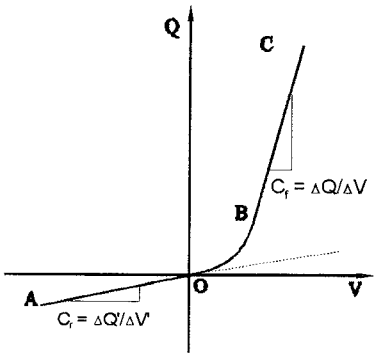


**Figure 2. Modified model of SRD.**

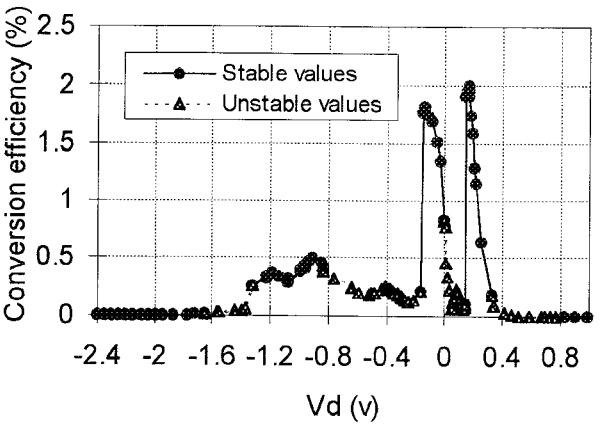


**Figure 5. Expermental results of conversion efficiency vs. bias voltage.**

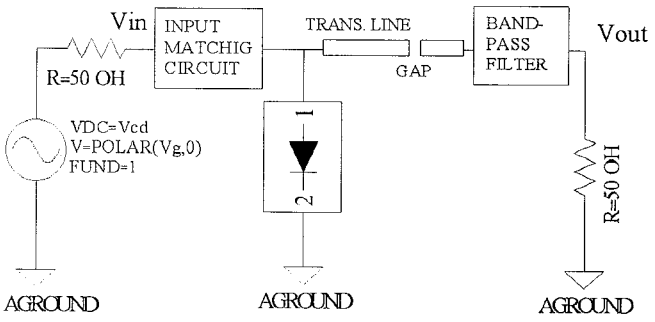


**Figure 3. Simulation circuit of SRD multiplier.**